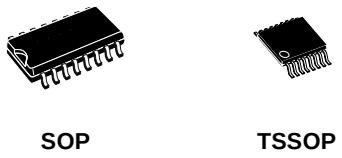
74LCX139

LOW VOLTAGE CMOS DUAL 2 TO 4 DECODER/DEMULTIPLEXER

- 5V TOLERANT INPUTS
- HIGH SPEED:
  t_{PD} = 6.2ns (MAX.) at V_{CC} = 3V
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 24mA (MIN) at V_{CC} = 3V
- PCI BUS LEVELS GUARANTEED AT 24 mA
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  V_{CC}(OPR) = 2.0V to 3.6V (1.5V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 139
- LATCH-UP PERFORMANCE EXCEEDS 500mA (JESD 17)
- ESD PERFORMANCE:
  HBM > 2000V (MIL STD 883 method 3015);
  MM > 200V



SOP **TSSOP**

Table 1: Order Codes

PACKAGE	T & R
SOP	74LCX139MTR
TSSOP	74LCX139TTR

DESCRIPTION

The 74LCX139 is a low voltage CMOS DUAL 2 TO 4 LINE DECODER/DEMULTIPLEXER fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology.
It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal environment for inputs.

The active low enable input can be used for gating or as a data input for demultiplexing applications. While the enable input is held high, all four outputs are high independently of the other inputs.
It has same speed performance at 3.3V than 5V AC/ACT family, combined with a lower power consumption.
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Figure 1: Pin Connection And IEC Logic Symbols

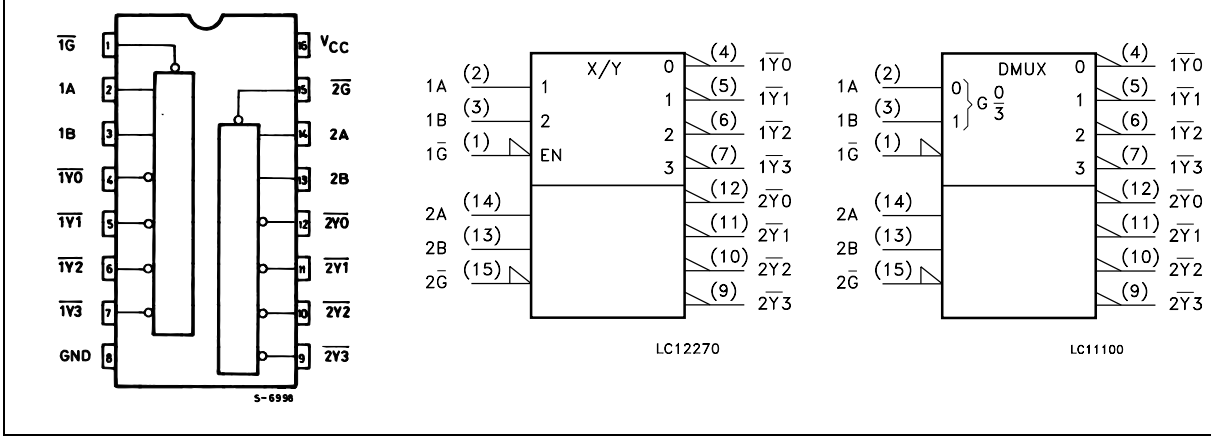


Figure 2: Input And Output Equivalent Circuit

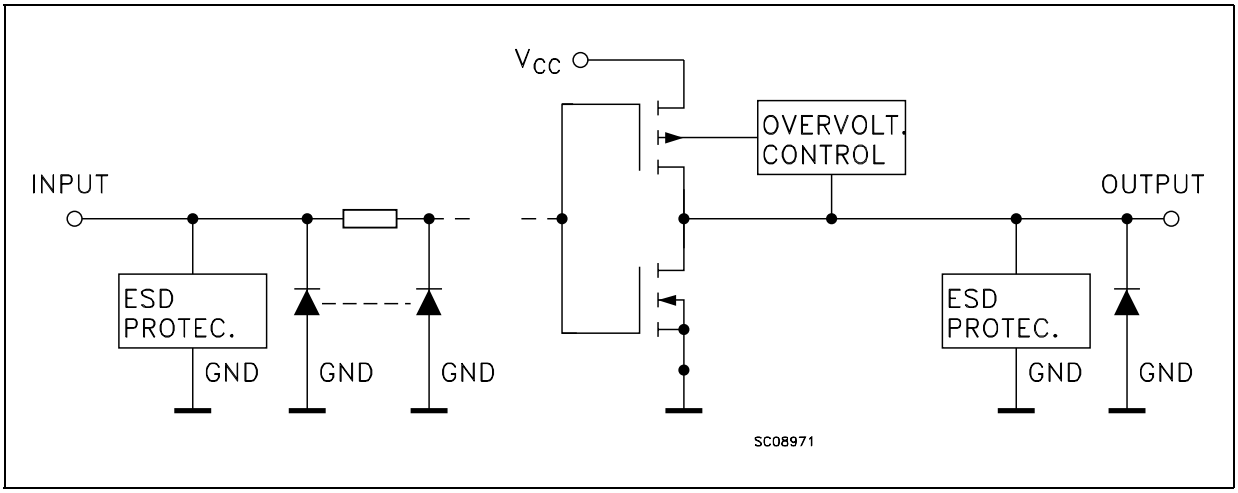


Table 2: Pin Description

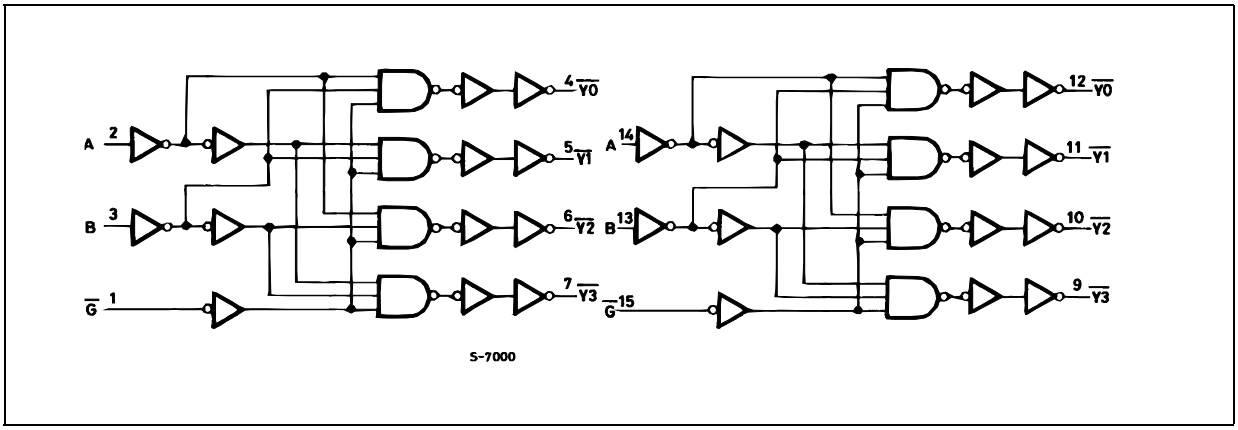
PIN N°	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{G}$, $2\overline{G}$	Enable Inputs
2, 3	1A, 1B	Address Inputs
4, 5, 6, 7	$1\overline{Y0}$ to $1\overline{Y3}$	Outputs
12, 11, 10, 9	$2\overline{Y0}$ to $2\overline{Y3}$	Outputs
14, 13	2A, 2B	Address Inputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

Table 3: Truth Table

INPUTS			OUTPUTS			
ENABLE	SELECT					
$\overline{G}$	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

X : Don't Care

Figure 3: Logic Diagram



This logic diagram has not be used to estimate propagation delays

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage (V_{CC} = 0V)	-0.5 to +7.0	V
V_O	DC Output Voltage (High or Low State) (note 1)	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 50	mA
I_{OK}	DC Output Diode Current (note 2)	- 50	mA
I_O	DC Output Current	± 50	mA
I_{CC}	DC Supply Current per Supply Pin	± 100	mA
I_{GND}	DC Ground Current per Supply Pin	± 100	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
1) I_O absolute maximum rating must be observed
2) V_O < GND

Table 5: Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2.0 to 3.6	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage (V_{CC} = 0V)	0 to 5.5	V
V_O	Output Voltage (High or Low State)	0 to V_{CC}	V
I_{OH}, I_{OL}	High or Low Level Output Current (V_{CC} = 3.0 to 3.6V)	± 24	mA
I_{OH}, I_{OL}	High or Low Level Output Current (V_{CC} = 2.7V)	± 12	mA
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 2)	0 to 10	ns/V

1) Truth Table guaranteed: 1.5V to 3.6V
2) V_{IN} from 0.8V to 2V at V_{CC} = 3.0V

Table 6: DC Specifications

Symbol	Parameter	Test Condition		Value				Unit
		V_{CC} (V)		-40 to 85 °C		-55 to 125 °C		
				Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.7 to 3.6		2.0		2.0		V
V_{IL}	Low Level Input Voltage				0.8		0.8	V
V_{OH}	High Level Output Voltage	2.7 to 3.6	I_O=-100 µA	V_{CC}-0.2		V_{CC}-0.2		V
		2.7	I_O=-12 mA	2.2		2.2		
		3.0	I_O=-18 mA	2.4		2.4		
			I_O=-24 mA	2.2		2.2		
V_{OL}	Low Level Output Voltage	2.7 to 3.6	I_O=100 µA		0.2		0.2	V
		2.7	I_O=12 mA		0.4		0.4	
		3.0	I_O=16 mA		0.4		0.4	
			I_O=24 mA		0.55		0.55	
I_I	Input Leakage Current	2.7 to 3.6	V_I = 0 to 5.5V		± 5		± 5	µA
I_{off}	Power Off Leakage Current	0	V_I or V_O = 5.5V		10		10	µA
I_{CC}	Quiescent Supply Current	2.7 to 3.6	V_I = V_{CC} or GND		10		10	µA
			V_I or V_O= 3.6 to 5.5V		± 10		± 10	
ΔI_{CC}	I_{CC} incr. per Input	2.7 to 3.6	V_{IH} = V_{CC} - 0.6V		500		500	µA

Table 4: DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Value			Unit
		V_{CC} (V)		T_A = 25 °C			
				Min.	Typ.	Max.	
V_{OLP}	Dynamic Low Level Quiet Output (note 1)	3.3	C_L = 50pF, V_{IL} = 0V, V_{IH} = 3.3V		0.8		V
V_{OLV}					-0.8		

1) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

Table 7: AC Electrical Characteristics

Symbol	Parameter	Test Condition				Value				Unit
		V_{CC} (V)	C_L (pF)	R_L (Ω)	t_s = t_r (ns)	-40 to 85 °C		-55 to 125 °C		
						Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time A, B to Y	2.7	50	500	2.5		7.3		7.3	ns
		3.0 to 3.6				1.0	6.2	1.0	6.2	
t_{PLH} t_{PHL}	Propagation Delay Time G to Y	2.7	50	500	2.5		5.8		5.8	ns
		3.0 to 3.6				1.0	5.3	1.0	5.3	
t_{OSLH} t_{OSHL}	Output To Output Skew Time (note1, 2)	3.0 to 3.6	50	500	2.5		1.0		1.0	ns

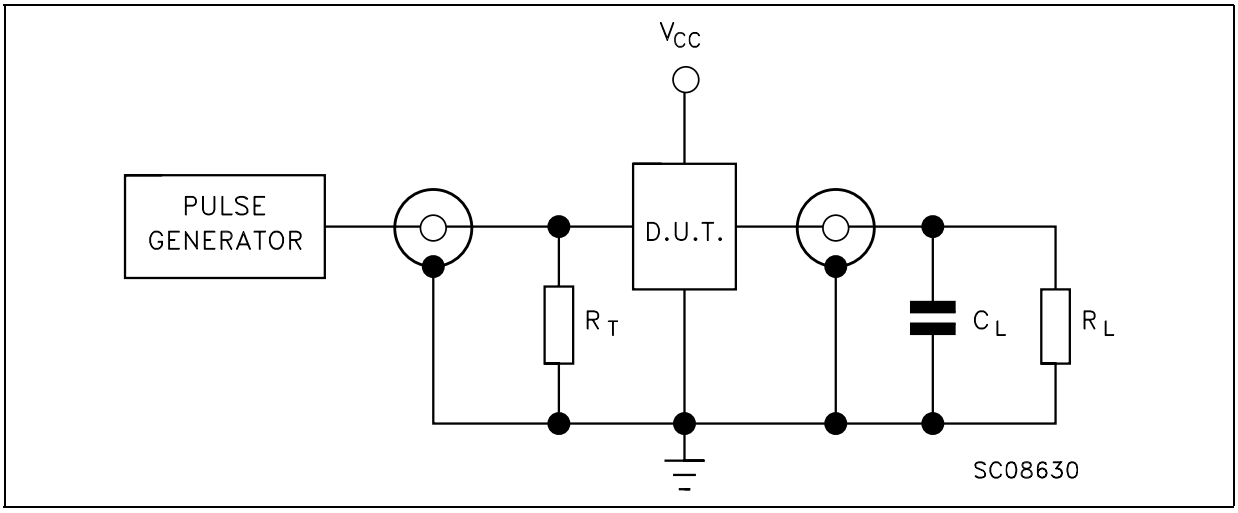
1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (t_{OSLH} = | t_{PLHm} - t_{PLHn}|, t_{OSHL} = | t_{PHLm} - t_{PHLn}|)
2) Parameter guaranteed by design

Table 8: Capacitive Characteristics

Symbol	Parameter	Test Condition		Value			Unit
		V_{CC} (V)		T_A = 25 °C			
				Min.	Typ.	Max.	
C_{IN}	Input Capacitance	3.3	V_{IN} = 0 to V_{CC}		6		pF
C_{PD}	Power Dissipation Capacitance (note 1)	3.3	f_{IN} = 10MHz V_{IN} = 0 or V_{CC}		26		pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2$ (per gate)

Figure 5: Test Circuit



C_L = 50 pF or equivalent (includes jig and probe capacitance)
R_L = 500Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

Figure 6: Waveform - Propagation Delays For Inverting Outputs (f=1MHz; 50% duty cycle)

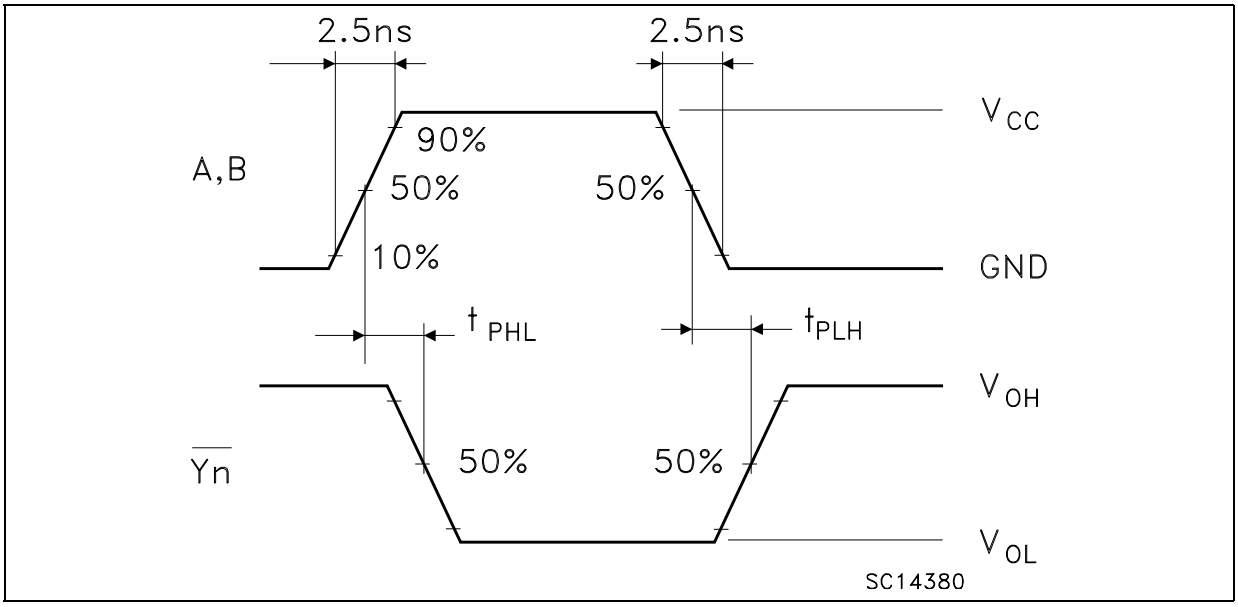
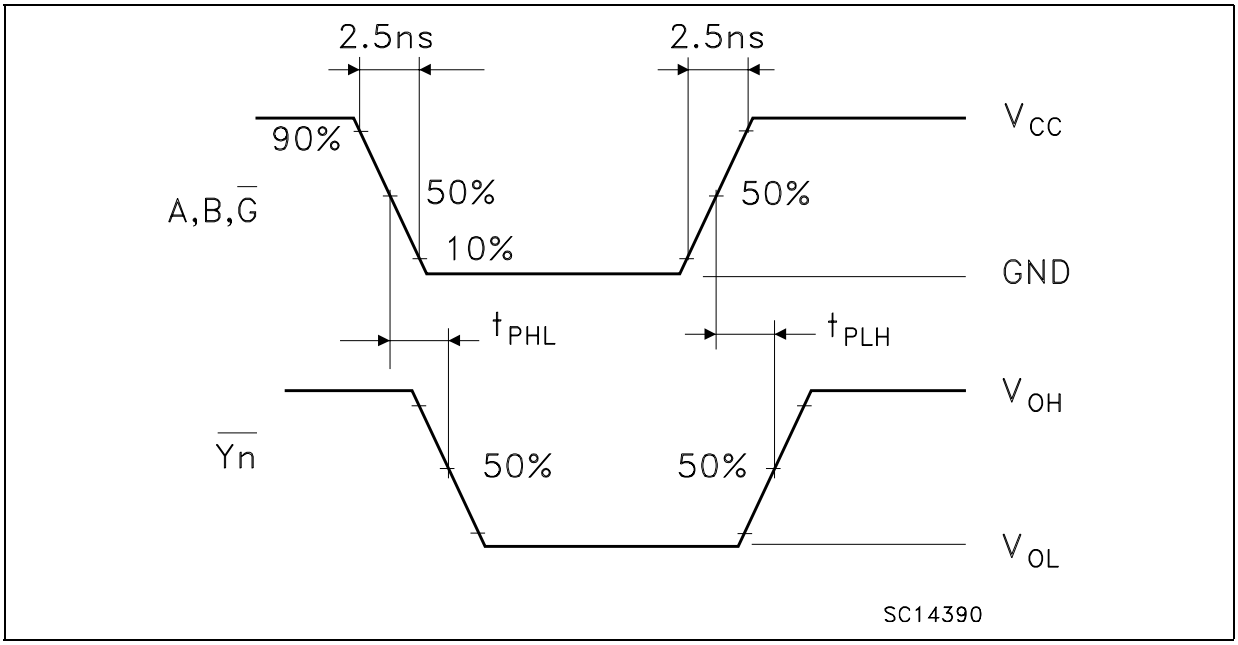
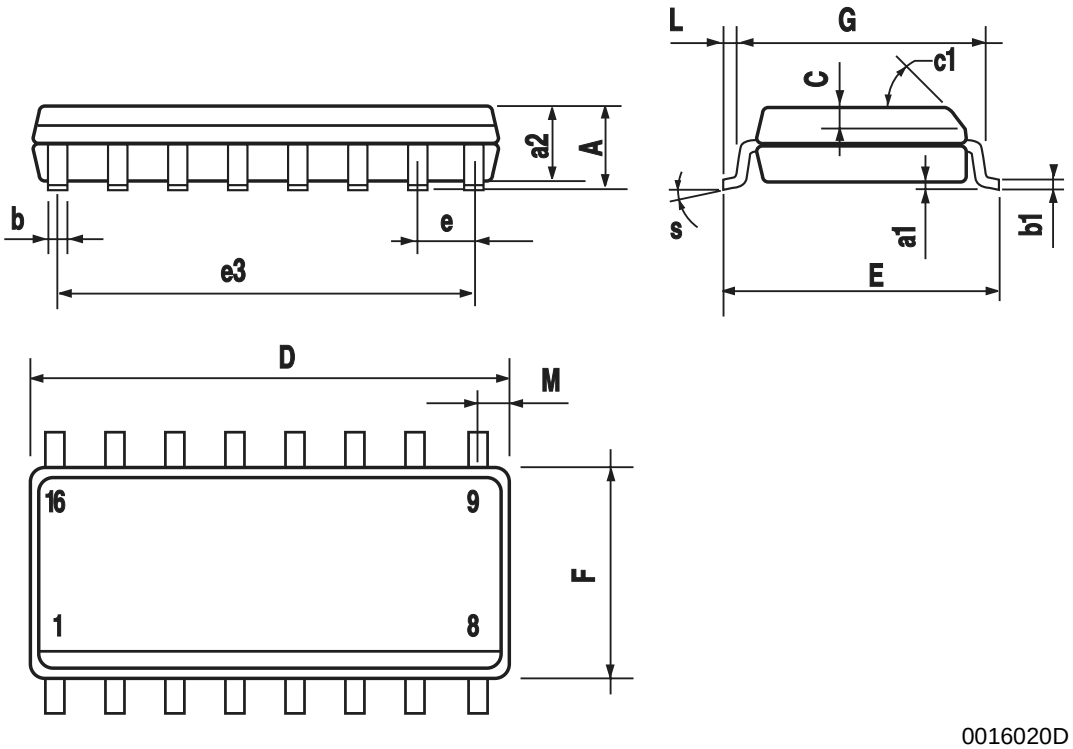


Figure 7: Waveform - Propagation Delays For Non-inverting Outputs (f=1MHz; 50% duty cycle)



SO-16 MECHANICAL DATA

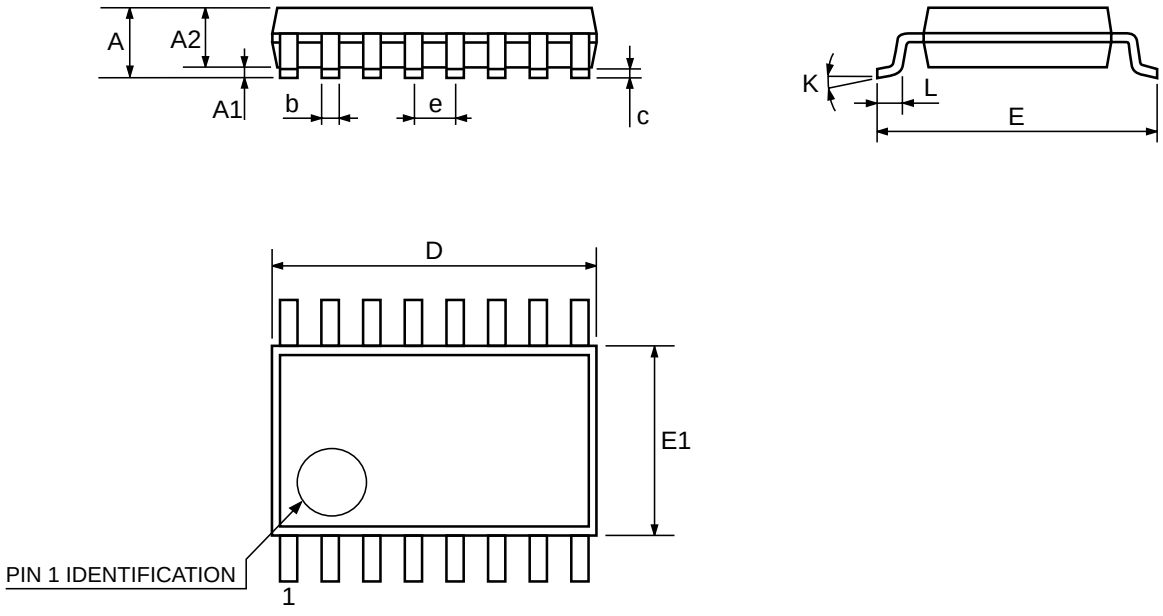
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.004		0.010
a2			1.64			0.063
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



0016020D

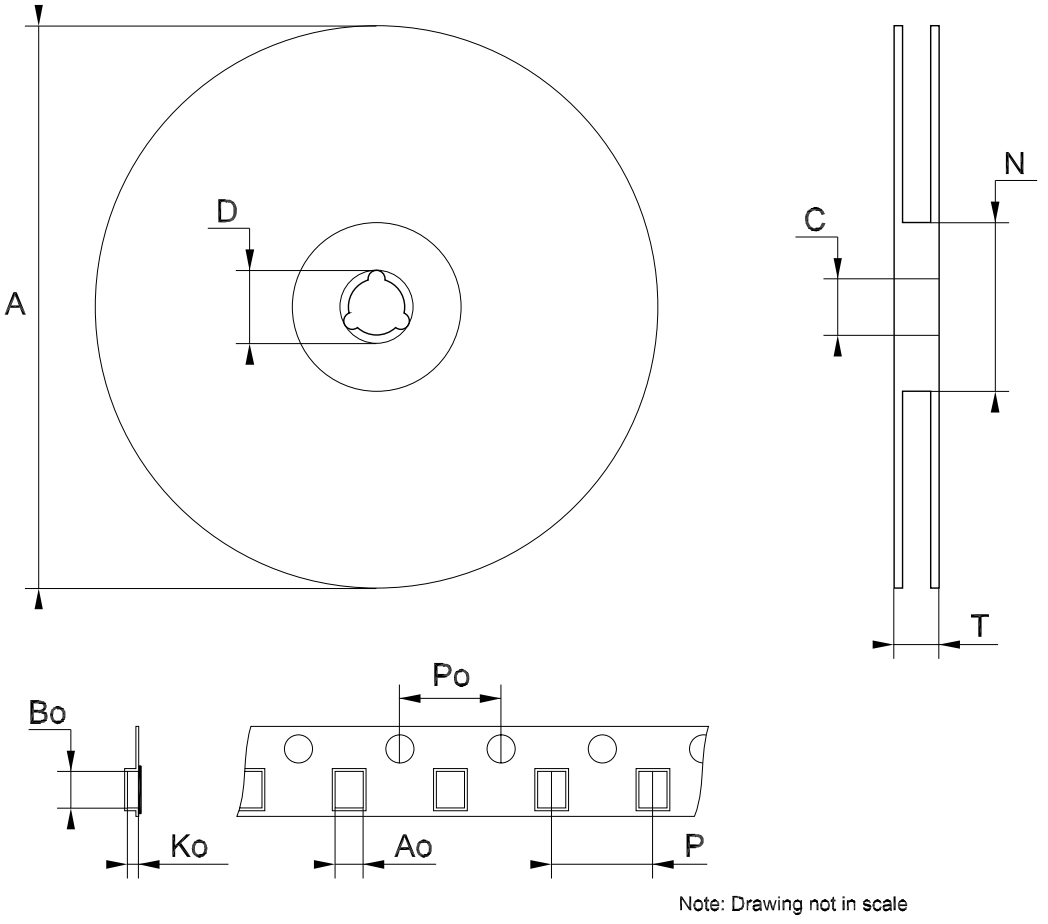
TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Tape & Reel SO-16 MECHANICAL DATA

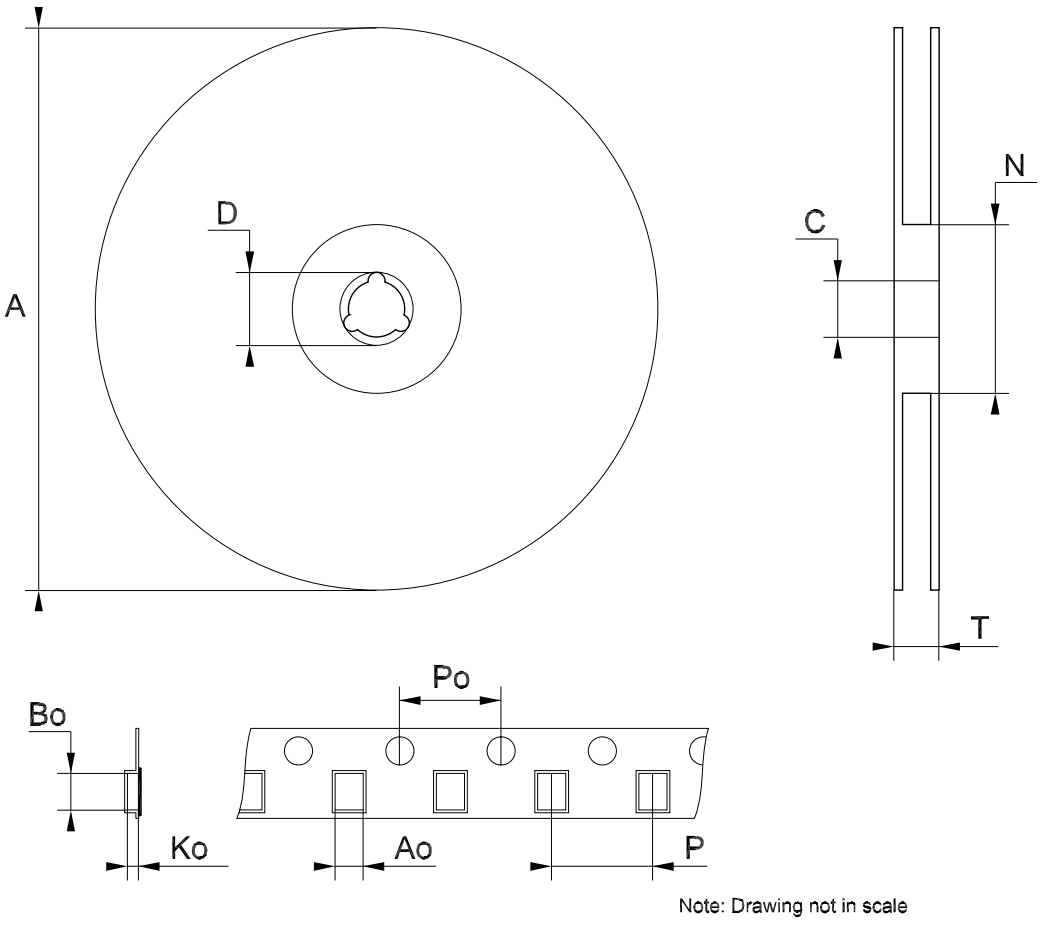
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.45		6.65	0.254		0.262
Bo	10.3		10.5	0.406		0.414
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale

Tape & Reel TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Bo	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale

Table 9: Revision History

Date	Revision	Description of Changes
15-Sep-2004	3	Ordering Codes Revision - pag. 1.